REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-15 are pending in the present application. Claims 1 and 9 are amended by the present amendment.

In the outstanding Office Action, Claims 1-15 were rejected under 35 U.S.C. § 112, second paragraph; Claims 1, 2, 5-10 and 13-15 were rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 5,006,980 to Sanders; and Claims 3, 4, 11 and 12 were rejected under § 103(a) as unpatentable over Sanders in view of U.S Patent No. 6,477,638 to Gearty and Hennessy, "Computer Organization and Design."

Regarding the rejection of Claims 1-15 under 35 U.S.C. § 112, second paragraph, Claims 1 and 9 are amended in light of comments in the outstanding Office Action. Accordingly, Applicant respectfully requests the rejection of Claims 1-15 under 35 U.S.C. § 112, second paragraph, be withdrawn.

In addition, Applicant respectfully traverses the rejection of Claims 1, 2, 5-10 and 13-15 under 35 U.S.C. § 102(e) as anticipated by Sanders.

Claim 1 is directed to a data processing apparatus configured to perform a pipeline processing by dividing a pipeline into a plurality of stages. The apparatus includes, in part, first and second pipeline processing portions that operate at different timings from each other, and the operational timing of a plurality of stages in theses pipeline processing portions can be controlled for each stage. Claim 9 includes similar features.

More specifically, a plurality of stages in the first pipeline processing portion is supplied with different control signals from each other, and each stage performs the processing operation based on the corresponding control signal. A plurality of control signals which latch and delay a plurality of control signals supplied to a plurality of stages in the first

pipeline processing portion is supplied to the respective stages in the second pipeline processing portion. Therefore, the stages in the first pipeline processing portion perform the processing at a timing faster than timings of the respective stages in the second pipeline processing portion.

Applicant respectfully submits that Sanders does not teach or suggest each feature of independent Claims 1 and 9. In particular, Sanders does not teach or suggest control signals having timings asynchronous to each other that are inputted to respective stages and does not teach or suggest performing a pipeline processing in a plurality of stages in sequence. Sanders describes inputting control input 28 in a first stage of latches connected in series, and latches the control input 28 in respective latches, in order. The outputs of the latches are supplied to the segments of the execution unit and the segments of a memory management unit. Thus, in Sanders, the latched control input outputted from a plurality of latches connected in series, synchronizes with a common pipeline-clock, and the respective latched control inputs are signals with phases one pipeline-clock behind. Therefore, Sanders indicates that the segments perform the processing operation within one clock unit of the pipeline-clock. That is, the operations of the segments, according to Sanders, are constrained in terms of time, and it is impossible to set the operational timing separate from the respective segments. Accordingly, Applicant respectfully submits that Sanders does not teach or suggest "performing said first pipeline processing in a plurality of stages in sequence based on a plurality of control signals . . . having timings asynchronous to each other," as recited in independent Claim 9, and as similarly recited in independent Claim 1.

Furthermore, Sanders indicates that the latches for controlling the execution unit and the latches for controlling the execution unit operate in parallel. The operational timing of the execution unit and the operational timing of the management unit are not staggered with respect to each other. Further, Sanders Fig. 12 indicates two kinds of latches that operate in

parallel to each other, and the outputs of the first kind of latches are latched by the second kind of latches. Accordingly, in the case of Sanders, the execution unit and the memory management unit operate in parallel. Therefore, in the apparatus of Sanders, if one segment in the execution unit sends data to the segment in the memory management unit, the operations of segments may cause conflict, and there is a likelihood of problems in that data transmission.

On the other hand, in the present invention, the control signal obtained by latching the control signal supplied to the respective stages in the first pipeline processing portion is supplied to the respective stages in the second pipeline processing portion. Thus, in the claimed invention, the first pipeline processing portion always operates faster in terms of timing than the second pipeline processing portion.

Accordingly, Applicant respectfully submits that independent Claims 1 and 9, and claims depending therefrom, are allowable.

In addition, Applicant respectfully traverses the rejection of Claims 3, 4, 11 and 12 under 35 U.S.C. § 103(a) as unpatentable over Sanders in view of Gearty and Hennessy.

Claims 3, 4, 11 and 12 depend from Claims 1 and 9, which as discussed above, are believed to be allowable. Further, Applicant respectfully submits that Gearty and Hennessy do not supply the claimed features lacking in the disclosure of Sanders. In particular, in Fig. 4, Gearty describes two pipelines and a latch circuit. However, Gearty does not teach or suggest that control signals are provided for each stage. Although Gearty uses the output of stage E3 as a control signal, no other control signal is described at all. Thus, Gearty and Hennessey neither teach nor suggest "control signals inputted to the respective stages," as recited in Claims 1 and 9.

Accordingly, Applicant respectfully requests the rejection of Claims 3, 4, 11 and 12 under 35 U.S.C. § 103(a) be withdrawn.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action that effect is respectfully requested.

Respectfully submitted,

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